What is claimed is:

1. A level shift circuit comprising:

a first transistor circuit which conducts a first node and a first power supply line when a second node is at a second power supply potential and does not conduct them when said second node is at a first power supply potential;

a second transistor circuit which conducts said second node and said first power supply line when said first node is at said second power supply potential and does not conduct them when said first node is at said first power supply potential;

a third transistor circuit which conducts said first node and said second power supply line when an input signal is at a first input potential and does not conduct them when said input signal is at a second input potential;

a fourth transistor circuit which conducts said second node and said second power supply line when said input signal is at a second input potential and does not conduct them when said input signal is at said first input potential; and

a fifth transistor circuit which switches a value of an inflow current or emission current of said second node or said first node according to a control signal, when said second node or said first node is conducted to both of said first power supply line and said second power supply line.

2. The level shift circuit according to Claim 1, wherein said first transistor circuit comprises a first conductive type first transistor one end of which is connected to said first power supply line, the other end of which is connected to said

first node, and control terminal of which is connected to said second node;

said second transistor circuit comprises a first conductive type second transistor one end of which is connected to said first power supply line, the other end of which is connected to said second node, and a control terminal of which is connected to said first node;

said third transistor circuit comprises a second conductive type third transistor one end of which is connected to said second power supply line, the other end of which is connected to said first node, and a control terminal of which inputs said input signal; and

said fourth transistor circuit comprises a second conductive type fourth transistor one end of which is connected to said second power supply line, the other end of which is connected to said second node, and a control terminal of which inputs an inverted value of said input signal.

3. The level shift circuit according to Claim 2, wherein said fifth transistor circuit comprises:

a second conductive type fifth transistor one end of which is connected to said second power supply line and a control terminal of which inputs said control signal; and

a second conductive type sixth transistor one end of which is connected to the other end of said fifth transistor, the other end of which is connected to said second node, and a control terminal of which inputs an inverted value of said input signal.

4. The level shift circuit according to Claim 2, wherein said fifth transistor circuit further comprises:

a second conductive type fifth transistor disposed between said second power supply line and said fourth transistor circuit, and a control terminal of which inputs said control signal; and

a second conductive type sixth transistor disposed between said second power supply line and said fourth transistor circuit, and a control terminal of which inputs an inverted value of said input signal.

5. The level shift circuit according to Claim 2, wherein said fifth transistor circuit comprises:

a second conductive type fifth transistor one end of which is connected to said second power supply line and a control terminal of which inputs said control signal;

a second conductive type sixth transistor one end of which is connected to the other end of said fifth transistor, the other end of which is connected to said first node, and a control terminal of which inputs said input signal;

a second conductive type seventh transistor one end of which is connected to said second power supply and a control terminal of which inputs said control signal; and

a second conductive type eighth transistor one end of which is connected to the other end of said seventh transistor, the other end of which is connected to said second node, and a control terminal of which inputs an inverted value of said input signal.

6. The level shift circuit according to Claim 2, wherein said fifth transistor comprises:

a second conductive type fifth transistor disposed between said second power supply line and said third transistor circuit, and a control terminal of which inputs said control signal;

a second conductive type sixth transistor disposed between said second power supply line and said third transistor circuit, and a control terminal of which inputs said input signal;

a second conductive type seventh transistor disposed between said second power supply line and said fourth transistor circuit, where said control signal is input from a control terminal; and

a second conductive type eighth transistor disposed between said second power supply line and said fourth transistor circuit, and a control terminal of which inputs an inverted value of said input signal.

7. The level shift circuit according to Claim 2, wherein said fifth transistor circuit comprises:

a first conductive type fifth transistor one end of which is connected to said first power supply line and a control terminal of which inputs said control signal; and

a first conductive type sixth transistor one end of which is connected to the other end of said fifth transistor, the other end of which is connected to said second node, and a control terminal of which is connected to said first node.

8. The level shift circuit according to Claim 2, wherein said fifth transistor circuit comprises:

a first conductive type fifth transistor disposed between said second transistor circuit and said first power supply line, and a control terminal of which inputs said control signal; and

a first conductive type sixth transistor disposed between said second transistor circuit and said first power supply line, and a control terminal of which is connected to said first node.

9. The level shift circuit according to Claim 2, wherein said fifth transistor circuit comprises:

a first conductive type fifth transistor one end of which is connected to said first power supply line and a control terminal of which inputs said control signal;

a first conductive type sixth transistor one end of which is connected to the other end of said fifth transistor, the other end of which is connected to said first node, and a control terminal of which is connected to said second node;

a first conductive type seventh transistor one end of which is connected to said first power supply line and a control terminal of which inputs said control signal; and

a first conductive type eighth transistor one end of which is connected to the other end of said seventh transistor, the other end of which is connected to said second node, and a control terminal of which is connected to said first node.

10. The level shift circuit according to Claim 2, wherein said fifth transistor circuit comprises:

a first conductive type fifth transistor disposed between said first transistor circuit and said first power supply line, and a control terminal of which inputs said control signal;

a first conductive type sixth transistor disposed between said first transistor circuit and said first power supply line, and a control terminal of which is connected to said second node;

a first conductive type seventh transistor disposed between said second transistor circuit and said first power supply line, and a control terminal of which inputs said control signal; and

a first conductive type eighth transistor disposed between said second transistor circuit and said first power supply line, and a control terminal of which is connected to said first node.

11. The level shift circuit according to Claim 2, wherein said fifth transistor circuit comprises:

a first conductive type fifth transistor one end of which is connected to said first power supply line and a control terminal of which inputs said control signal; and

a first conductive type sixth transistor one end of which is connected to the other end of said fifth transistor, the other end of which is connected to said second node, and a control terminal of which inputs an inverted value of said input signal.

12. The level shift circuit according to Claim 2, wherein said fifth transistor circuit comprises:

a first conductive type fifth transistor one end of which is connected to said first power supply line, and a control terminal of which inputs said control signal;

a first conductive type sixth transistor one end of which is connected to the other end of said fifth transistor, the other end of which is connected to said second node, and a control terminal of which inputs an inverted value of said input signal;

a first conductive type seventh transistor disposed between said first transistor circuit and said first power supply line,

and a control terminal of which inputs an inverted value of said control signal; and

a first conductive type eighth transistor disposed between said second transistor circuit and said first power supply line, and a control terminal of which inputs an inverted value of said control signal.

13. The level shift circuit according to Claim 2, wherein said fifth transistor circuit comprises:

a first conductive type fifth transistor one end of which is connected to said first power supply line and a control terminal of which inputs said control signal;

a first conductive type sixth transistor one end of which is connected to the other end of said fifth transistor, the other end of which is connected to said second node, and a control terminal of which inputs an inverted value of said input signal;

a first conductive type seventh transistor one end of which is connected to said first power supply line, the other end of which is connected to said first node, and a control terminal of which inputs said control signal; and

a second conductive type eighth transistor disposed between said third transistor circuit and said first node, and a control terminal of which inputs said control signal.

14. The level shift circuit according to Claim 1, wherein said first transistor circuit comprises a first conductive type first transistor one end of which is connected to said first power supply line and a control terminal of which is connected to said second node, and a first conductive type second transistor

one end of which is connected to the other end of said first transistor, the other end of which is connected to said first node, and a control terminal of which inputs said input signal;

said second transistor circuit comprises a first conductive type third transistor one end of which is connected to said first power supply line and a control terminal of which is connected to said first node, and a first conductive type fourth transistor one of which is connected to the other end of said forth transistor, the other end of which is connected to said second node, and a control terminal of which inputs an inverted value of said input signal;

said third transistor circuit comprises a second conductive type fifth transistor one end of which is connected to said second power supply line, the other end of which is connected to said first node, and a control terminal of which inputs said input signal; and

said fourth transistor circuit comprises a second conductive type sixth transistor one end of which is connected to said second power supply line, the other end of which is connected to said second node, and a control terminal of which inputs an inverted value of said input signal.

15. The level shift circuit according to Claim 14, wherein said fifth transistor circuit comprises:

a second conductive type seventh transistor one end of which is connected to said second power supply line and a control terminal of which inputs said control signal; and

a second conductive type eighth transistor one end of which is connected to the other end of said seventh transistor, the other end of which is connected to said second node, and a control terminal of which inputs an inverted value of said input signal.

16. The level shift circuit according to Claim 14, wherein said fifth transistor circuit comprises:

a second conductive type seventh transistor disposed between said second power supply line and said fourth transistor circuit, and a control terminal of which inputs said control signal; and

a second conductive type eighth transistor disposed between said second power supply line and said fourth transistor circuit, and a control terminal of which inputs an inverted value of said input signal.

17. The level shift circuit according to Claim 14, wherein said fifth transistor circuit comprises:

a second conductive type seventh transistor one end of which is connected to said second power supply line and a control terminal of which inputs said control signal;

a second conductive type eighth transistor one end of which is connected to the other end of said seventh transistor, the other end of which is connected to said first node, and a control terminal of which inputs said input signal;

a second conductive type ninth transistor where one end is connected to said second power supply line and said control signal is input from a control terminal; and

a second conductive type tenth transistor where one end is connected to the other end of said ninth transistor, the other end

is connected to said second node, and a control terminal inputs an inverted value of said input signal.

18. The level shift circuit according to Claim 14, wherein said fifth transistor circuit comprises:

a second conductive type seventh transistor disposed between said second power supply line and said third transistor circuit, and a control terminal of which inputs said control signal;

a second conductive type eighth transistor disposed between said second power supply line and said third transistor circuit, and a control terminal of which inputs said input signal;

a second conductive type ninth transistor disposed between said second power supply line and said fourth transistor circuit, and a control terminal of which inputs said control signal; and

a second conductive type tenth transistor disposed between said second power supply line and said fourth transistor circuit, and a control terminal of which inputs an inverted value of said input signal.

19. The level shift circuit according to Claim 14, wherein said fifth transistor circuit comprises:

a first conductive type seventh transistor one end of which is connected to said first power supply line and a control terminal of which inputs said control signal; and

a first conductive type eighth transistor one end of which is connected to the other end of said seventh transistor, the other end of which is connected to said second node, and a control terminal of which is connected to said first node.

20. The level shift circuit according to Claim 14, wherein said fifth transistor circuit comprises:

a first conductive type seventh transistor disposed between said second transistor circuit and said first power supply line, and a control terminal of which inputs said control signal; and

a first conductive type eighth transistor disposed between said second transistor circuit and said first power supply line, and a control terminal of which is connected to said first node.

21. The level shift circuit according to Claim 14, wherein said fifth transistor circuit comprises:

a first conductive type seventh transistor one end of which is connected to said first power supply line and a control terminal of which inputs said control signal;

a first conductive type eighth transistor, one end of which is connected to the other end of said seventh transistor, the other end of which is connected to said first node, and a control terminal of which is connected to said second node;

a first conductive type ninth transistor one end of which is connected to said first power supply line and a control terminal of which inputs said control signal; and

a first conductive type tenth transistor one end of which is connected to the other end of said ninth transistor, the other end of which is connected to said second node, and a control terminal of which is connected to said first node.

22. The level shift circuit according to Claim 14, wherein said fifth transistor circuit comprises:

a first conductive type seventh transistor disposed between said first transistor circuit and said first power supply line, and a control terminal of which inputs said control signal;

a first conductive type eighth transistor disposed between said first transistor circuit and said first power supply line, and a control terminal of which is connected to said second node;

a first conductive type ninth transistor disposed between said second transistor circuit and said first power supply line, and a control terminal of which inputs said control signal; and

a first conductive type tenth transistor disposed between said second transistor circuit and said first power supply line, and a control terminal of which is connected to said first node.

23. The level shift circuit according to Claim 14, wherein said fifth transistor circuit comprises a first conductive type seventh transistor one end of which is connected to said first power supply line, the other end of which is connected to said one end of said third transistor, and a control terminal of which inputs said control signal.

24. The level shift circuit according to Claim 14, wherein said fifth transistor circuit comprises:

a first conductive type seventh transistor one end of which is connected to said first power supply line, the other end of which is connected to said one end of said third transistor, and a control terminal of which inputs said control signal; and

a first conductive type eighth transistor disposed between said first transistor circuit and said first power supply line,

and a control terminal of which inputs an inverted value of said control signal.

25. The level shift circuit according to Claim 14, wherein said fifth transistor circuit comprises:

a first conductive type seventh transistor one end of which is connected to said first power supply line, the other end of which is connected to said one end of said third transistor, and a control terminal of which inputs said control signal;

a first conductive type eighth transistor one end of which is connected to said first power supply line, the other end of which is connected to said first node, and a control terminal of which inputs said control signal; and

a second conductive type ninth transistor disposed between said third transistor circuit and said first node, and a control terminal of which inputs said control signal.